What is claimed is:

1. A double data rate memory device, comprising:

a first memory array;

a second memory array;

a mux control adapted to receive control signals;

a first pipeline coupled to the first memory array and the second memory array, wherein the first pipeline passes data from one of the first memory array and the second memory array and through the first pipeline on a rising edge of an external clock;

a second pipeline coupled to the first memory array and the second memory array, wherein the second pipeline passes data from the first memory array and the second memory array and through the second pipeline on a falling edge of the external clock;

wherein the first pipeline further comprises a first data mux connected to the mux control, the first memory array and the second memory array, the first data mux being adapted to direct data from one of the first memory array and the second memory array to the first pipeline; and

wherein the second pipeline further comprises a second data mux connected to the mux control, the first memory array and the second memory array, the second data mux being adapted to direct data from one of the first memory array and the second memory array to the second pipeline.

2. The memory device of claim 1, wherein mux control is adapted to receive address signals and clock signals.

3. The memory device of claim 1, wherein the first pipeline includes a plurality of latches.

4. The memory device of claim 3, wherein the second pipeline includes a further plurality of latches.

5. The memory device of claim 1, wherein the mux control determines which of the first pipeline and the second pipeline data from the first and second arrays is placed on.

6. The memory device of claim 1, wherein the first pipeline further comprises a first delay lock loop latch.

7. The memory device of claim 6, wherein the second pipeline further comprises a second delay lock loop latch.

8. The memory device of claim 7, wherein the at least one of the first latch and the second latch is operated by the mux control.

9. A double data rate memory device, comprising:

a first memory array;

a second memory array;

a control unit;

a first pipeline coupled to the control unit, the first memory array and the second memory array, wherein the first pipeline passes data from one of the first memory array and the second memory array and through the first pipeline on a rising edge of an external clock;

a second pipeline coupled to the control unit, the first memory array and the second memory array, wherein the second pipeline passes data from the first memory array and the second memory array and through the second pipeline on a falling edge of the external clock; and

wherein the control unit signals the first and second pipelines to pass data based on latency and clock cycle time.

10. The memory device of claim 9, wherein the first pipeline and the second pipeline include a first plurality of latches and a second plurality of latches, respectively.

11. The memory device of claim 9, wherein the first pipeline further comprises a first delay lock loop latch.

12. The memory device of claim 11, wherein the second pipeline further comprises a second delay lock loop latch.

13. The memory device of claim 12, wherein the at least one of the first latch and the second latch is operated by the mux control.

14. A double data rate memory device, comprising:

a first memory array;

a second memory array;

a first pipeline coupled to the first memory array and the second memory array, wherein the first pipeline passes data from one of the memory array and the second memory array and through the first pipeline on a rising edge of an external clock;

a second pipeline coupled to the first memory array and the second memory array, wherein the second pipeline passes data from one of the first memory array and the second memory array and through the second pipeline on a falling edge of the external clock;

a control unit connected to the first and second pipelines; and

wherein the control unit generates an internal clock.

15. The memory device of claim 14, wherein the first pipeline includes a first plurality of stages, the second pipeline includes a second plurality of stages, and wherein the control unit controls the passing of data among the stages of the first and second pipelines.

16. An integrated circuit, comprising:

a first array of memory cells having first data;

a second array of memory cells having second data;

a first pipeline operable for outputting data on a rising edge of a clock, the first pipeline having a first data mux connected to the first array and a first latch;

a second pipeline, in parallel with the first pipeline, operable for outputting data on a falling edge of the clock, the second pipeline having a second data mux connected to the second array and a second latch;

a data mux controller connected to the first and second data muxes to direct the first data to the first pipeline and to direct the second data to the second pipeline; and

wherein the first data mux is further connected to the second array.

17. The integrated circuit of claim 16, further comprising a control unit connected to the first pipeline and the second pipeline, wherein the control unit synchronizes the output of data with the clock by utilizing propagation time of the pipelines.

18. The integrated circuit of claim 16, wherein the first and second arrays are physically located in a memory array.

19. The integrated circuit of claim 16, wherein the first array is physically located separately from the second array.

20. The integrated circuit of claim 16, wherein the first pipeline further comprises at least two latches connected in series.

21. The integrated circuit of claim 20, wherein the second pipeline further comprises at least two latches connected in series.

22. The integrated circuit of claim 21, wherein the second data mux is further connected to the first array.

23. An integrated circuit, comprising:

a first array of memory cells having first data;

a second array of memory cells having second data;

a first pipeline operable for outputting data on a rising edge of a clock, the first pipeline having a first data mux connected to the first array and a first latch;

a second pipeline, in parallel with the first pipeline, operable for outputting data on a falling edge of the clock, the second pipeline having a second data mux connected to the second array and a second latch;

a data mux controller connected to the first and second data muxes to direct the first data to the first pipeline and to direct the second data to the second pipeline;

wherein the first data mux is further connected to the second array; and

an output buffer connected to the first and second pipeline.

24. The integrated circuit of claim 23, wherein the first pipeline further comprises at least two latches connected in series.

25. The integrated circuit of claim 24, wherein the second pipeline further comprises at least two further latches connected in series.

26. The integrated circuit of claim 23, wherein the output buffer is adapted to receive data on the rising edge of a clock and the falling edge of a clock.

27. The integrated circuit of claim 26, wherein the output buffer is adapted to output data to at least one of a processor and a disk drive.

28. The integrated circuit of claim 23, wherein the first pipeline further comprises a first delay lock loop latch, and wherein the second pipeline further comprises a second delay lock loop latch.

29. The integrated circuit of claim 28, wherein the at least one of the first latch and the second latch is operated by the data mux controller.

30. The integrated circuit of claim 23, wherein a rising edge latch operates on a rising edge of an internal clock and a falling edge latch operates on a falling edge of the internal clock, the internal clock operates in advance of the clock.

31. An integrated circuit comprising:

a first memory array;

a second memory array;

a first pipeline, having a first data mux connected to the first memory array and the second memory array, for outputting data on a rising edge of a clock;

a second pipeline, having a second data mux connected to the first memory array and the second memory array, for outputting data on a falling edge of the clock; and

a data mux controller connected to the first and second data muxes to direct data from the first memory array and the second memory array to the first pipeline and the second pipeline.

32. An integrated circuit comprising:

a first memory array;

a second memory array;

a first pipeline having a first data mux connected to the first memory array and the second memory array, at least one first latch connected in series to the first data mux, and a first delay lock loop latch connected to the first latch;

a second pipeline having a second data mux connected to the first memory array and the second memory array, at least one second latch connected in series to the second data mux and a second delay lock loop latch connected to the second latch;

a data mux controller connected to the first and second data muxes to direct first data to the first pipeline and second data to the second pipeline; and

a control unit, having an internal clock, connected to the first and second pipelines, to synchronize output of data with rising and falling edges of an external clock.

33. The integrated circuit of claim 32, wherein the data mux controller is adapted to simultaneously direct first data to the first pipeline and second data to the second pipeline.

34. The integrated circuit of claim 32, wherein the control unit signals the first delay lock loop latch to pass first data to an output buffer and signals the second delay lock loop latch to pass second data to an output buffer.

35. The integrated circuit of claim 32, wherein the control unit, having an internal clock, connected to the first and second pipelines, to synchronize output of data with rising and falling edges of an external clock.

36. A method for reading data from a memory device having a storage unit, a first pipeline and a second pipeline comprising:

selecting data in a storage unit, wherein the data includes first data and second data;

directing the first data to the first pipeline;

directing the second data to the second pipeline;

passing the first data from the first pipeline to an output buffer for output on a rising edge of a clock; and

passing the second data from the second pipeline to the output buffer for output on a falling edge of the clock.

37. A method comprising:

passing a first piece of data from a storage unit through a first mux to a first latch and passing a second piece of data from the storage unit through a second mux to a second latch;

on a first signal, passing the first piece through the first latch to a third latch and passing the second piece through the second latch to a fourth latch;

on a second signal, passing the first piece of data through the third latch to a fifth latch and passing the second piece through the fourth latch to a sixth latch;

on a third signal, passing the second piece of data through the sixth latch; and

on a fourth signal, passing the first piece of data through the fifth latch.

38. A method comprising:

selecting a first piece of data and a second piece of data;

passing the first piece of data to a first pipeline;

passing the second piece of data to a second pipeline;

outputting the first piece of data from the first pipeline on a first event; and

outputting the second piece of data from the second pipeline on a second event.

39. A method for reading data from a memory device having a storage unit, a first pipeline and a second pipeline comprising:

determining on which pipeline to place data from the storage unit;

passing a first half of the data to the first pipeline;

passing a second half of the data to a second pipeline;

outputting the first half of the data from the first pipeline on rising edges of an external clock; and

outputting the second half of the data from the second pipeline on falling edges of the external clock.

40. A method for reading data comprising:

issuing a read command;

selecting the data in a storage unit;

passing each piece of the data to a first or second pipeline alternatingly; and

outputting the data on rising and falling edges of a clock.

41. A method of operating a computer system comprising:

requesting data from a memory device having a storage unit and two parallel pipelines;

passing the data from the storage unit onto the pipelines; and

outputting the data from the pipelines to a processor at double data rate.

42. A method for controlling a memory device having two pipelines, the pipelines having at least one latch connected in series, comprising:

determining latency and cycle time;

generating an internal clock which is advance of an external clock by utilizing the latency and the cycle time;

signaling the latches of the pipelines to pass data through the pipeline; and

outputting data from the pipelines synchronous to the external clock.

43. A method for controlling a memory device have a plurality of pipelines each having at least one strobe latch and one delay lock loop latch comprising:

determining latency and cycle time for the memory device;

generating an internal clock which is advance of an external clock by utilizing the latency and the cycle time;

signaling the at least one strobe latch on an offset from the external clock;

signaling the delay lock loop latch on an offset from the internal clock; and

outputting data from the plurality of pipelines.